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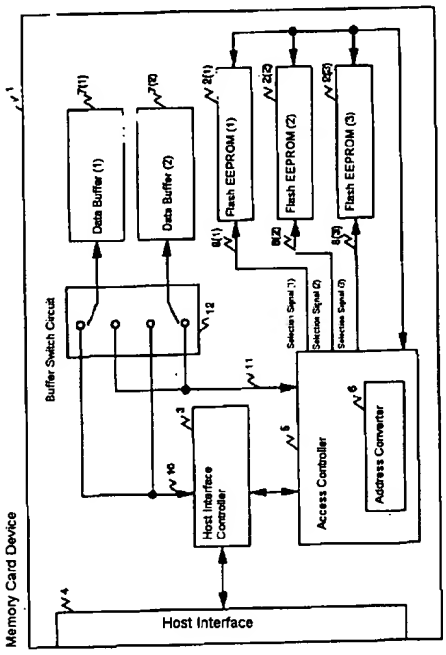
(54) [Title of the Invention] MEMORY CARD DEVICE

(57) [Abstract]

[Purpose] To provide a memory card device whose write speed does not slow down even when the capacity of a data buffer is insufficient.

[Constitution] Multiple data buffers 7 and a buffer switch circuit 12 which switches the data buffers 7 via the control of an access controller 5 are provided in a memory card device 1 which has the data buffers 7.
[Effects] Due to the fact that the multiple data buffers 7 are alternately switched by the buffer switch circuit 12, and that the date reading from the host CPU and writing from the data buffers 7 to a flash-type EEPROM 2 are simultaneously performed, no standby operation except for waiting for erasure occurs.

Figure 1



[Claims]
[Claim 1] A memory card device comprising: multiple flash-type EEPROMs under control of a higher-order control unit; a host communication method that reads and writes data under control of said higher-order control unit; a flash-type EEPROM control method that decodes an address or command read in through said host communication method; an address conversion method which is present within said flash-type EEPROM control method and converts the addresses in order to simultaneously read and write said flash-type EEPROMs; and a temporary memory method which temporarily stores the data read in through said host communication method, characterized by the fact that multiple units of said temporary memory method are provided, and that a switching method which switches said temporary memory methods under control of said flash-type EEPROM control method is provided.
[Detailed Explanation of the Invention]
[0001]
[Industrial Field of Application] The present invention relates to a memory device, and especially to control of data writing to the flash-type EEPROM.
[0002]
[Prior Art] Since a memory card device using the flash-type EEPROM does not require a power source to hold data, it is used a new memory card device replacing the memory card devices using SRAM or DRAM, and has a constitution shown in Figure 2, for example.
[0003] Here, the flash-type EEPROM2 within the memory card device 1 has fixed minimum units for the data handled at the time of writing or erasure, and the data are handled in a single batch equivalent to those units. The following explanation assumes that the erasure unit is 3 times the size of the writing unit, but it is not limited as such.
[0004] When writing the write data to the flash-type EEPROM 2 (1) or 2(3) within the memory card device 1 through the host interface 4, the host interface controller 3 writes the address information and the size of data transfer transferred via the host interface 4 into the access controller 5. The host interface controller 3 next transfers the write data sent via the host interface 4 to the access controller 5. The access controller 5 stores the write data sent from the host interface controller 3 in the data buffer 7. Here, the data buffer 7 has a capacity equal to or larger than that which can be obtained when a single erasure operation is performed in each of the flash-type EEPROMs 2.
[0005] In order to write the write data stored in the data buffer 7 to the flash-type EEPROM 2 (1) or 2 (3) at high speed, the speed gain was conventionally aimed at by controlling the Selection Lines 8 (1) or 8 (3) using the address converter circuit 6 within the access controller 5 so that the multiple flash-type EEPROMs 2 (1) and 2 (3) could be simultaneously accessed, as indicated by JP Tokkai H6-119128,
[0006] Figure 3 shows the flow when the data are written from the data buffer 7 to the flash-type EEPROM 2 (1) or 2 (3). As indicated by Figure 3, because it is possible to transfer the data to the flash-type EEPROM 2 (2) while the data are being written to the flash-type EEPROM 2 (1), it is possible to write faster than when the data are written by transferring them to each of the flash-type EEPROM 2 (1) or 2 (3).
[0007]
[The Problem that the Invention is to Solve] Although it is possible to write at high speed using the conventional method as mentioned above, when the data buffer 7 is not able to obtain the capacity equal to or larger than that obtained by a single erasure operation in each of the flash-type EEPROMs 2, the writing speed drops due to the occurrence of a standby operation, as shown in Figure 4 ($T1 < T2$). Nevertheless, with a small and think device such as a memory card device, the necessary buffer capacity cannot always be obtained.
[0008]The purpose of the present invention is provide a memory card device that does not experience the drop in writing speed even when the sufficient data buffer capacity cannot be obtained.
[0009]
[Means for Solving the Problem] In order to solve the above-mentioned problem, the present invention provides a memory card device comprising: multiple flash-type EEPROMs under control of a higher-order control unit; a host communication method that reads and writes data under control of said higher-order control unit; a flash-type

EEPROM control method that decodes an address or command read in through said host communication method; an address conversion method which is present within said flash-type EEPROM control method and converts the addresses in order to simultaneously read and write said flash-type EEPROMs; and a temporary memory method which temporarily stores the data read in through said host communication method, wherein multiple units of said temporary memory method are provided, and a switching method which switches said temporary memory methods under control of said flash-type EEPROM control method is provided.

[0010]

[Effects] According to the present invention, even when the capacity of the temporary memory method cannot equal or exceed the capacity obtainable when a single erasure operation is performed in each of the flash-type EEPROMs, the multiple temporary methods alternately switch via the switch method, with the data reading from the higher-order control unit and data writing from the temporary memory method to the flash-type EEPROM being simultaneously performed, and thus no standby operation except for waiting for erasure occurs.

[0011]

[Embodiment] Figure 1 is a block diagram showing the first embodiment in the present invention, and Figure 5 is an explanatory diagram showing the operation of the embodiment.

[0012] In Figure 1, 1 is the memory card device in the present invention; 2 is the flash-type EEPROM within the memory card device 1; 3 is the host interface controller that sets the command and address sent from the host CPU and the like via the host interface 4 to the access controller 5; 5 is the access controller that decodes the address or command read in via the host interface controller and controls the read-write of the flash-type EEPROMs; 6 is the address converter circuit that converts the address in order to simultaneously read and write the flash-type EEPROM; 7 is the date buffer that temporarily stores the data read in via the host interface controller 3; 8 is the selection signal that controls the flash-type EEPROM 2; 12 is the buffer switch circuit that switches the data buffers 7 (1) and 7 (2) according to the instructions from the access controller 5.

[0013] When the data are written from the host CPU to the flash-type EEPROM 2, the host CPU sets the write address, size of the write data, and the write command to the host interface controller 3 via the host interface 4. The host interface controller 3 sets the write address, the size of the write data, and the write command to the access controller 5.

[0014] The access controller 5 decodes the command thus set, and prior to the write operation, erases the address to be written once and only once in the amount of the erasure unit for each of the flash-type EEPROM 2 (1) or 2 (3). In the meantime, the write data are set in the data buffer 7 (1) and data buffer 7 (2) via the host interface controller 3. After the completion of erasure, the write address is set in the address converter circuit 6, and the selection signal 8 is put out in order to write the data to the flash-type EEPROM 2.

[0015] Next, the access controller 5 controls the buffer switch 12, so that the data bus 11 connects with the data buffer 7 (1), and that the data bus 10 connects with the data buffer 7 (2). Then, a data transfer from the data buffer 7 (1) to the flash-type EEPROM 2 (1) is performed under control of the access controller 5, and the write command is issued after the end of the transfer. The flash-type EEPROM 2 (1) hereby begins the writing operation.

[0016] Next, the access controller 5 controls the buffer switch circuit 12 so that the data bus 10 connects with the data buffer 7 (1), and that the data bus 11 connects with the data buffer 7 (2). Then, a data transfer from the data buffer 7 (2) to the flash-type EEPROM 2 (2) is performed under control of the access controller 5, and the write command is issued after the end of the transfer. The flash-type EEPROM 2 (2) hereby begins the writing operation. At this time, the host interface controller 3 simultaneously writes the next write date to the data buffer 7 (1) via the host interface 4. By repeating these operations, it becomes possible to write the write data into every erased block without causing any standby operation, as shown in Figure 5.

[0017] The present embodiment is characterized by the fact that, in the memory

card device, there are multiple data buffers 7, and that it has a buffer switch circuit 12 that switches the data buffers 7 under control of the access controller 5.

[0018]

[Effects of the Invention] In the present invention, even when the capacity of the buffers 7 cannot equal or exceed the capacity obtainable when a single erasure operation is performed in each of the flash-type EEPROMs 2, the multiple data buffers 7 alternately switch via the buffer switch method, with the data reading from the host CPU and data writing from the data buffers 7 to the flash-type EEPROM 2 being simultaneously performed, and thus no standby operation except for waiting for erasure occurs.

[0019] As such, the write speed does not slow down even when it is not possible to obtain a sufficient capacity for the data buffer.

[0020] Moreover, the capacity for the data buffer is small, and this can reduce the circuit scale.

[Brief Explanation of Drawings]

[Figure 1] A block diagram showing the schematic constitution of the memory card device of one embodiment in the present invention.

[Figure 2] A block diagram showing the schematic constitution of the memory card device of prior art.

[Figure 3] An explanatory diagram of the operation of an example of prior art.

[Figure 4] An explanatory diagram of the problem of an example of prior art.

[Figure 5] An explanatory diagram of the operation of the embodiment.

[Explanation of Reference Numerals]

1...Memory card device, 2...Flash-type EEPROM, 3...Host interface controller, 5...Access controller, 6...Address switch circuit, 7...Data buffer, 8...Selection signal, 12...Buffer switch circuit.

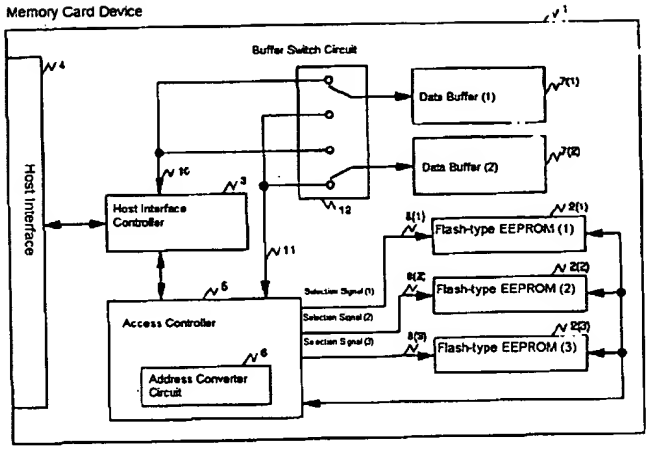


Figure 1

Figure 2

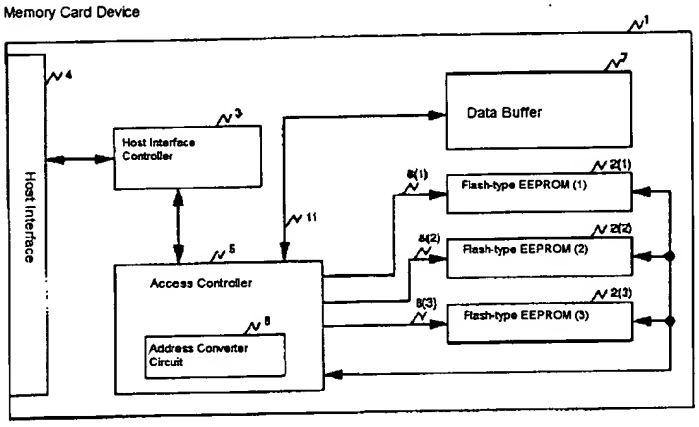


Figure 2

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Figure 3

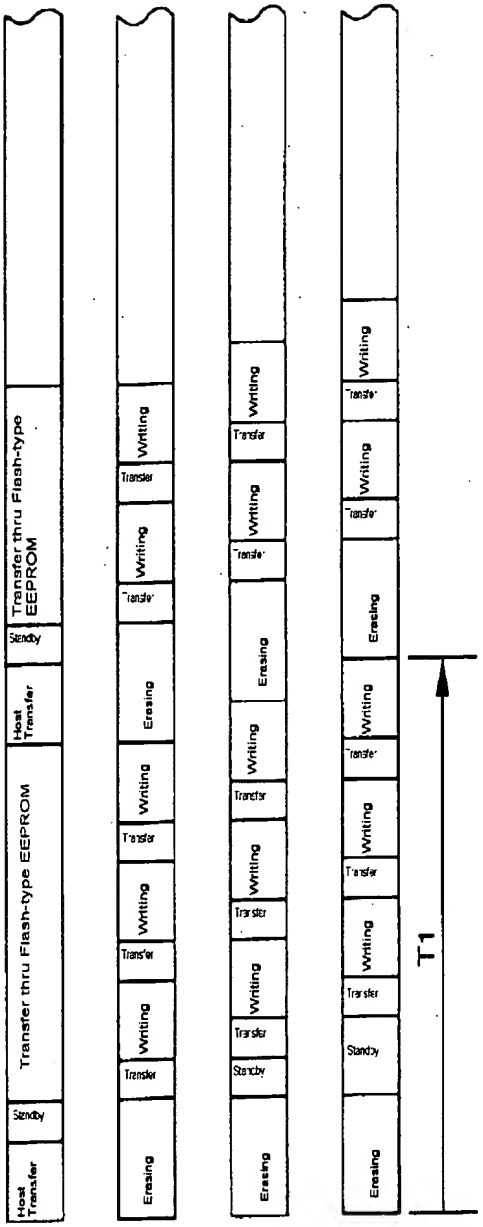
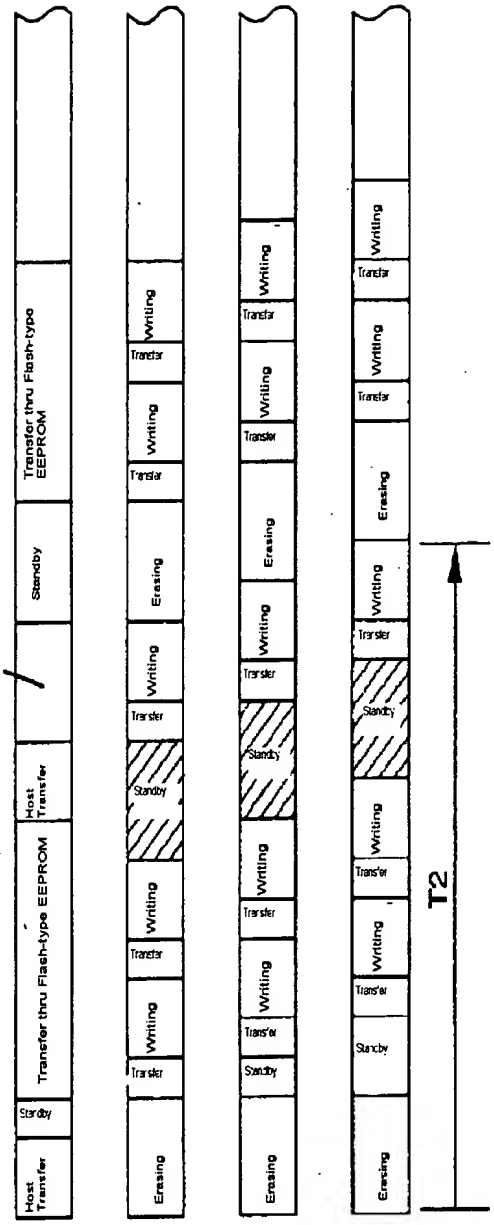


Figure 4



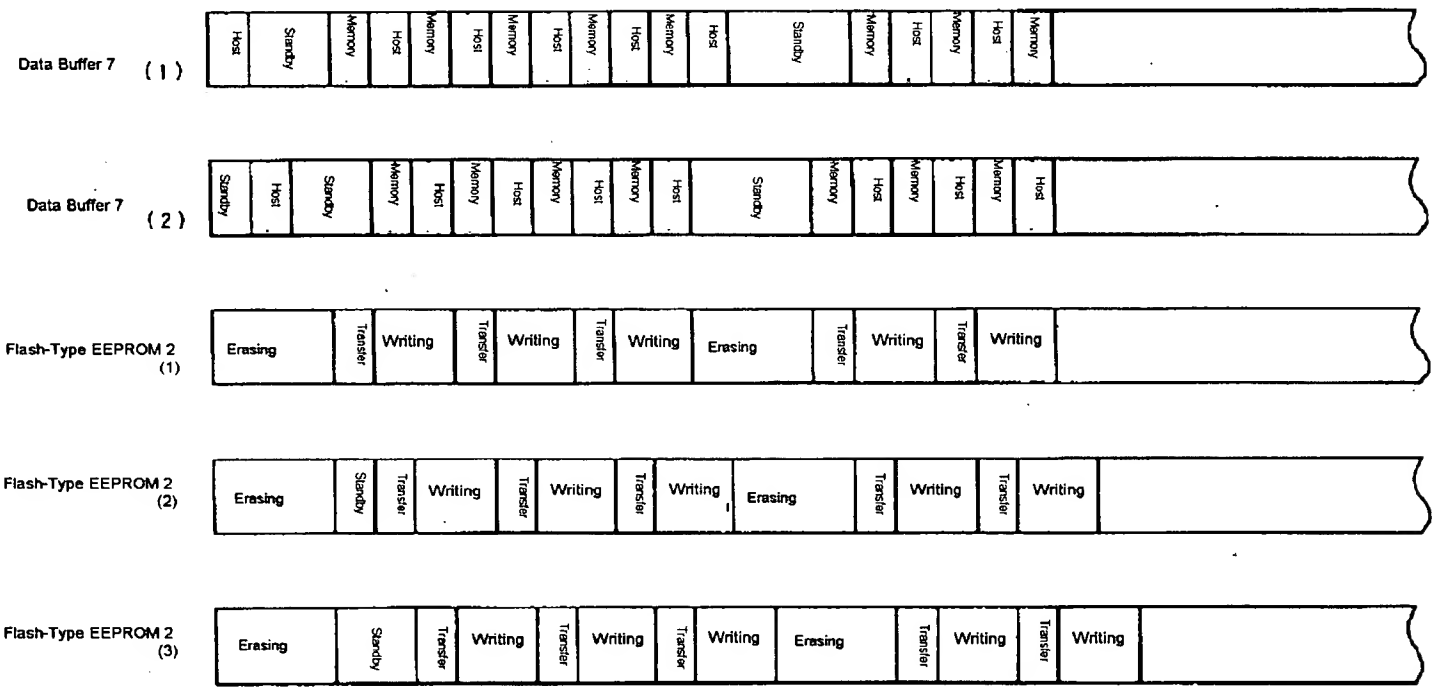


Figure 5

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